Memory Solutions for Diverging Applications

A New Perspective on Performance

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Agenda

- **Changing perspective of memory performance and development**
- **Performance trends and solutions in:**
  - Handheld/wireless
  - Networking
  - Graphics/entertainment
  - Servers
  - Laptops
  - Desktop PCs
- **Summary**

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Memory Performance – A Historical Perspective

- **One memory technology served nearly all applications**
  - Customers optimized their system designs to use the highest-volume memory device
  - Performance was improved over time by increasing clock rates
- **Slow data rates allowed system implementation using simple digital design techniques**
- **Customer engineering departments provided the majority of expertise needed for system implementation**
- **Supplier technical support focused on expertise in device features and protocol**

Memory Performance – Today's Perspective

- **Increasing emphasis on latency, bandwidth, and power dissipation – mutually exclusive priorities**
  - Segmentation of the memory market
- **Increased priority on innovation**
  - Decreased priority to use standard memory device in some applications
- **More complex memory requirements are demanding more engineering resources from suppliers and customers**
- **Ability to innovate and drive new technology is limited to the strongest players**

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Priorities for Memory Applications

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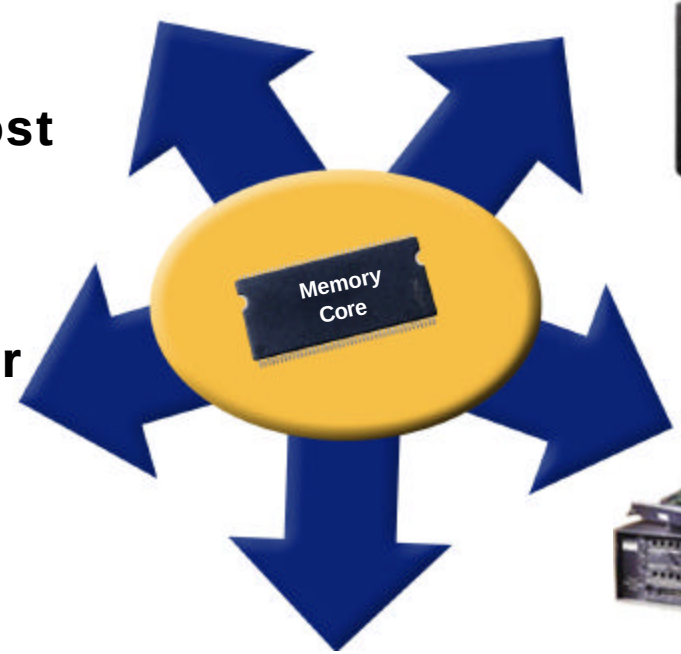
Desktop
Bandwidth
Volume / cost

Consumer / Entertainment
Very high bandwidth
Thermal / cost



Notebook
Small form factor
Low power
Thermal
Volume / cost

Network
Low latency
High bandwidth
Low power

Server
Density
Low power
Thermal
Desktop leverage

Handheld / Wireless
Small packaging
Very low power
Moderate cost

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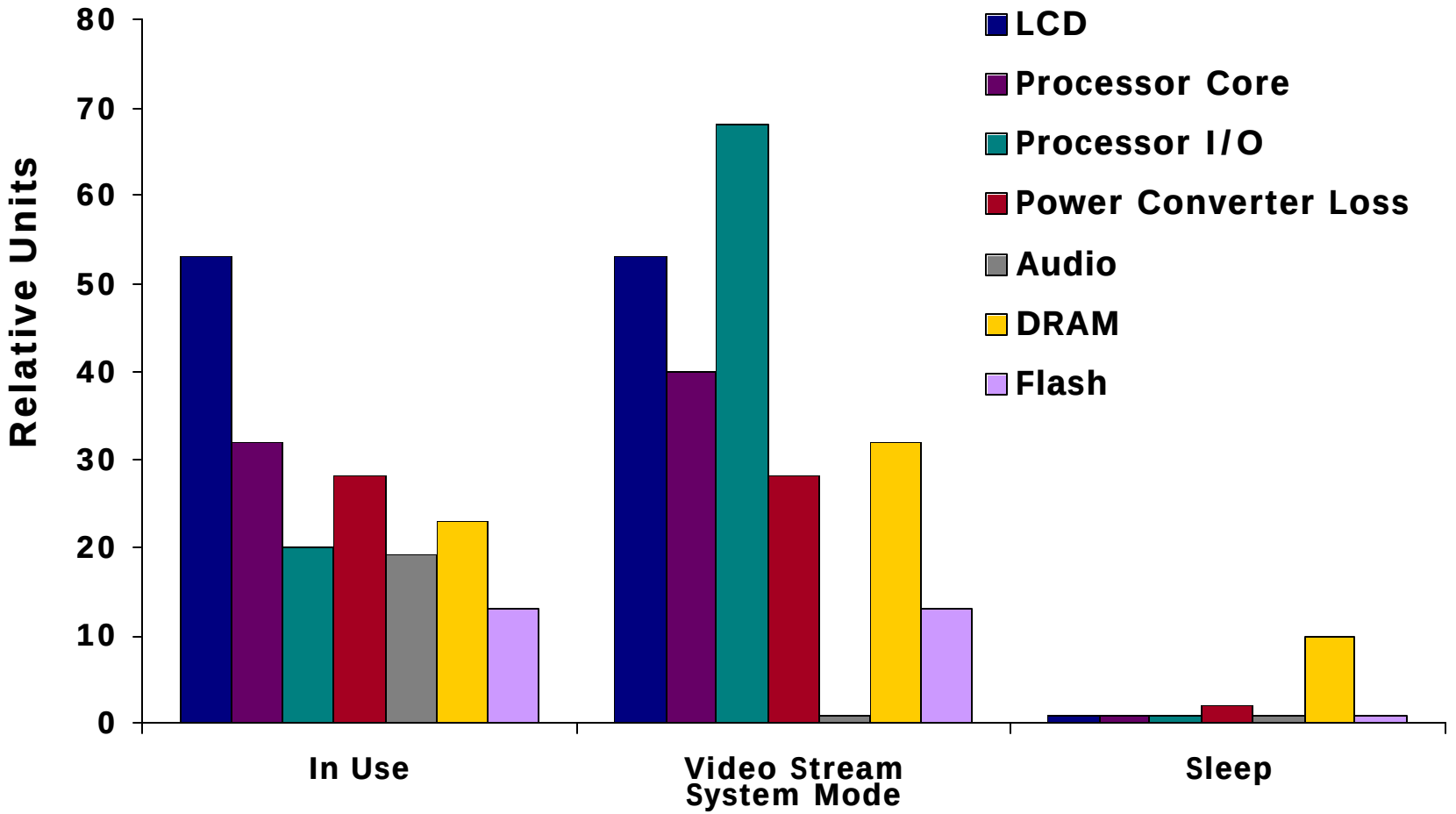
Handheld Power Usage



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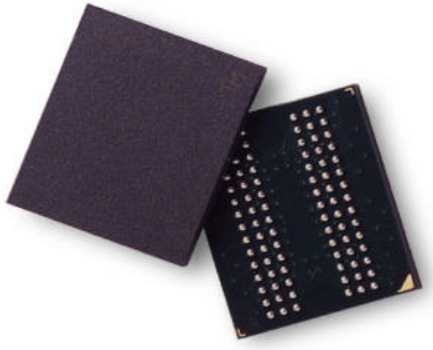
Handheld Solution – Mobile SDRAM

- **Lower operating voltage to reduce power dissipation in all operating modes**
- **Reduced standby (sleep) power by adding new operating modes**
  - Partial array self refresh
  - Temperature compensated refresh
- **Overall power reduction**
  - Operating >40%
  - Standby/self refresh >80%, but even greater when partial array mode is used!
- **Small form factor packaging**
  - FBGA and bare die



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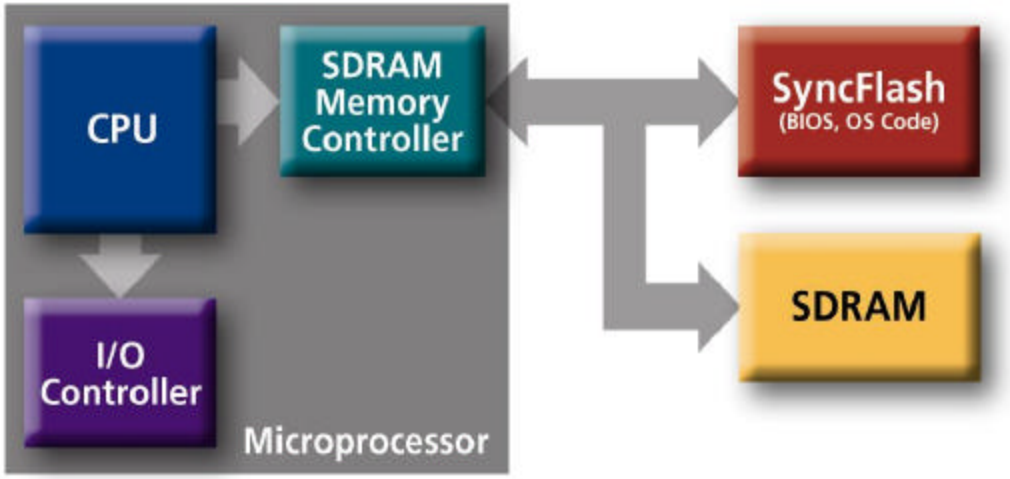
Instant-On for Handhelds

- **Solution: SyncFlash®**
  - NOR Flash with SDRAM-compatible interface
  - Resides on SDRAM bus
  - Direct boot from SyncFlash eliminates boot ROM
  - Execute-in-place at 133 MHz
  - System ready in 1-2 seconds!

Native SyncFlash Controller



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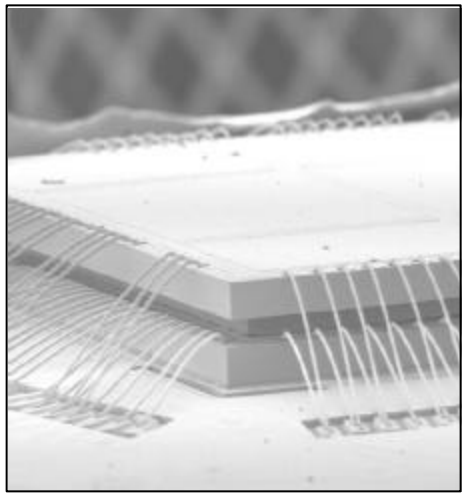
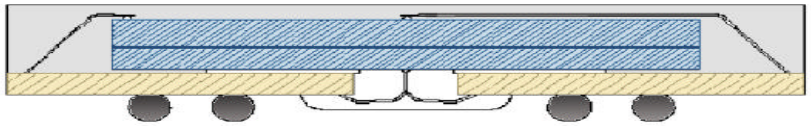
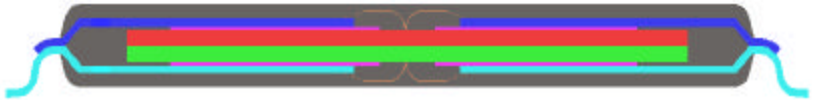
Handheld Solution - Packaging Options



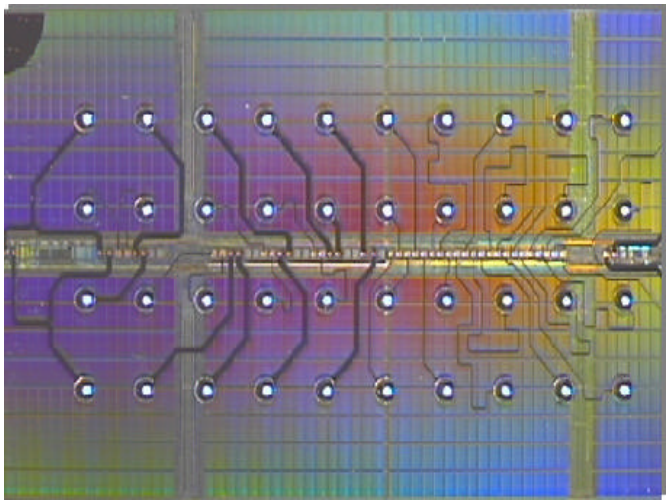
Same-Size Stacked Die



2BOC (FBGA)



2SOP



Wafer Level Re-distribution Layer

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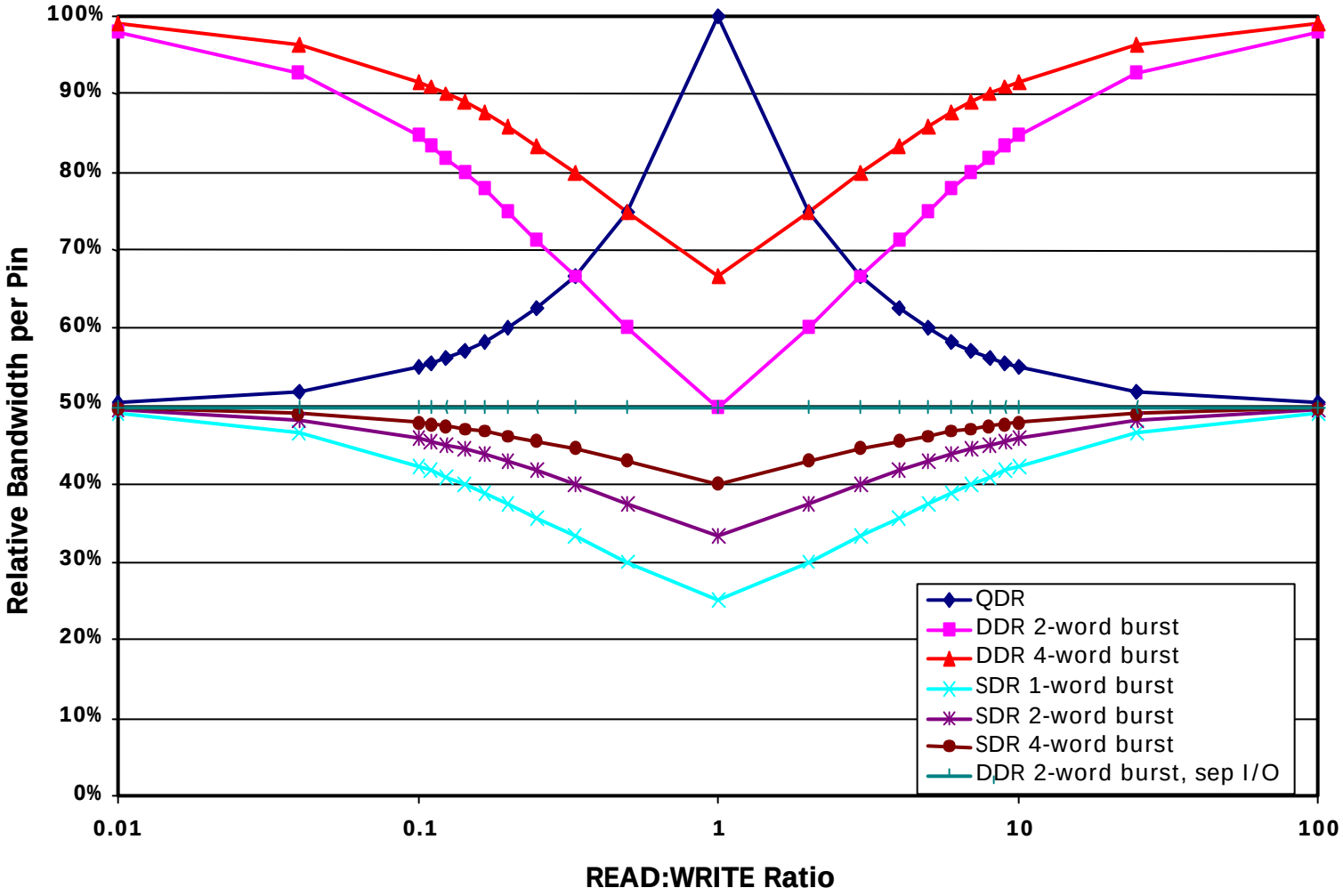
Network Performance



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Network Solution – New DRAM Architectures

- **SRAM devices used in networking designs are high cost per megabit**
- **New DRAM architectures: RLDRAM™ and FCRAM**
- **RLDRAM (Reduced Latency DRAM)**
  - Low random bank cycle or ^{t}RC for data bus efficiency
  - High bandwidth (800 Mb/s)
  - Low core and I/O voltages for power concerns
  - Minimized package size for space considerations
- **Future trends**
  - Higher bandwidth, lower latency, bare die, and stacked die packaging

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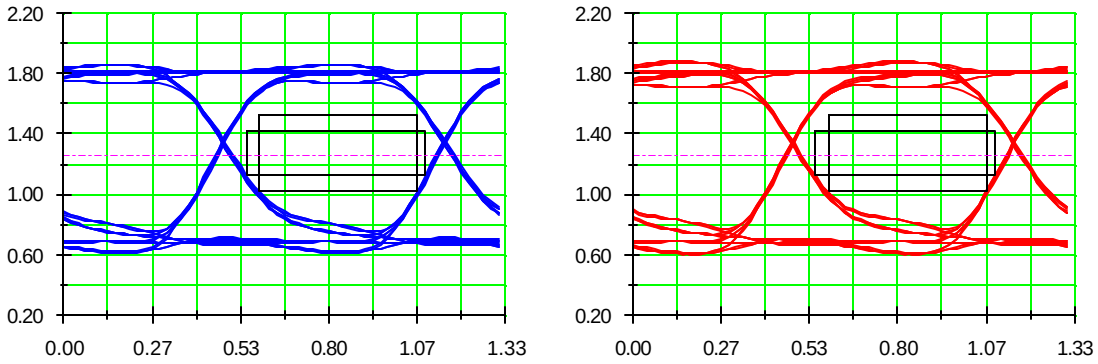
Network Solution - Ternary CAMs

- **What do TCAMs do ?**
  - Search all memory locations at exactly the same time
  - Provide network line cards with lightning-quick searches in hardware vs. slower software searches of conventional memory
- **Binary CAMs store only 0s and 1s – "Exact Match" searches**
- **TCAMs store 0s, 1s, and Xs (don't care)**
  - Group addresses into a single table entry
  - "Longest Prefix Match" searches

Graphics/Entertainment

- **Challenge: very high bandwidth, relatively low cost**
- **Solution: GDDR3**
  - x32 organization
  - New signaling interface
  - On-die termination
  - Flip-chip packaging
  - Ultra-high bandwidth – 1.0 Gb/s to 1.5 Gb/s



GDDR3 at 1.5 Gb/s

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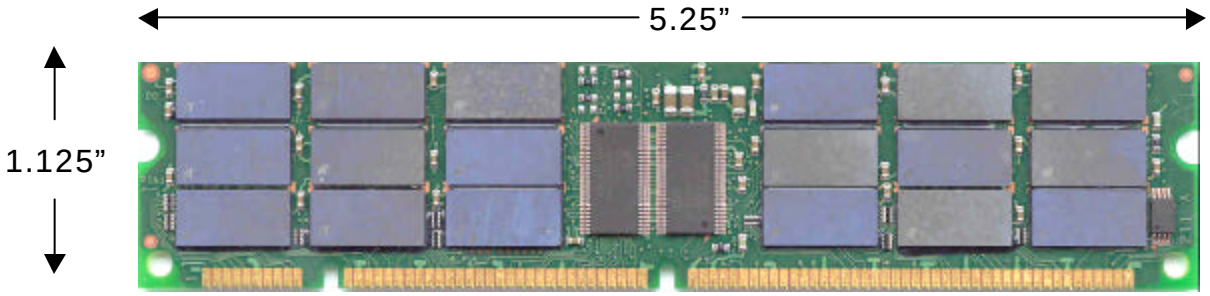
Servers

- **Challenge:**
  - Lower standby and operating power due to number of devices in system
    - Memory design challenge
  - High data rates require lower inductance packaging; low-profile DIMMs required for rack servers
  - How to build stacked modules?
- **Solution: 2BOC and flip-chip**



1GB Flip Chip Stacked Module

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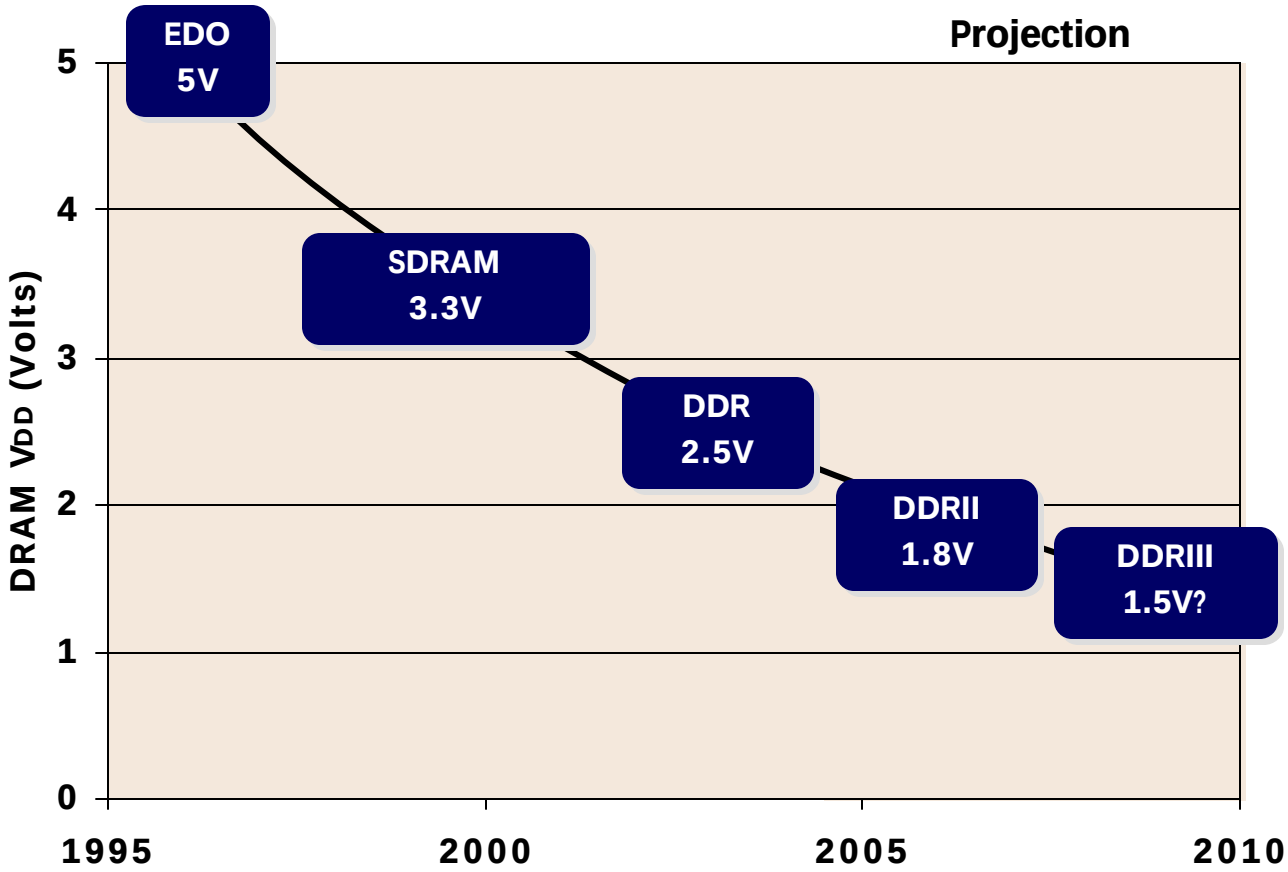
Laptops

- **Challenge: Low power, small form factor, low price**
- **Solution:**
  - DDRII
    - SODIMMs populated with FBGA components
    - 1.8V operating and I/O voltages
      - Power dissipation at 400 Mb/s is reduced by 20% over DDR266
    - On-die termination reduces system components and board real estate
    - Data rates increase to 400 Mb/s and 533 Mb/s

FBGA-Based, Small-Outline DIMM

Main Memory Voltages



- VDD is being reduced with each new technology
- I/O voltages are also being reduced
- Each decrease of VDD allows significant power reductions

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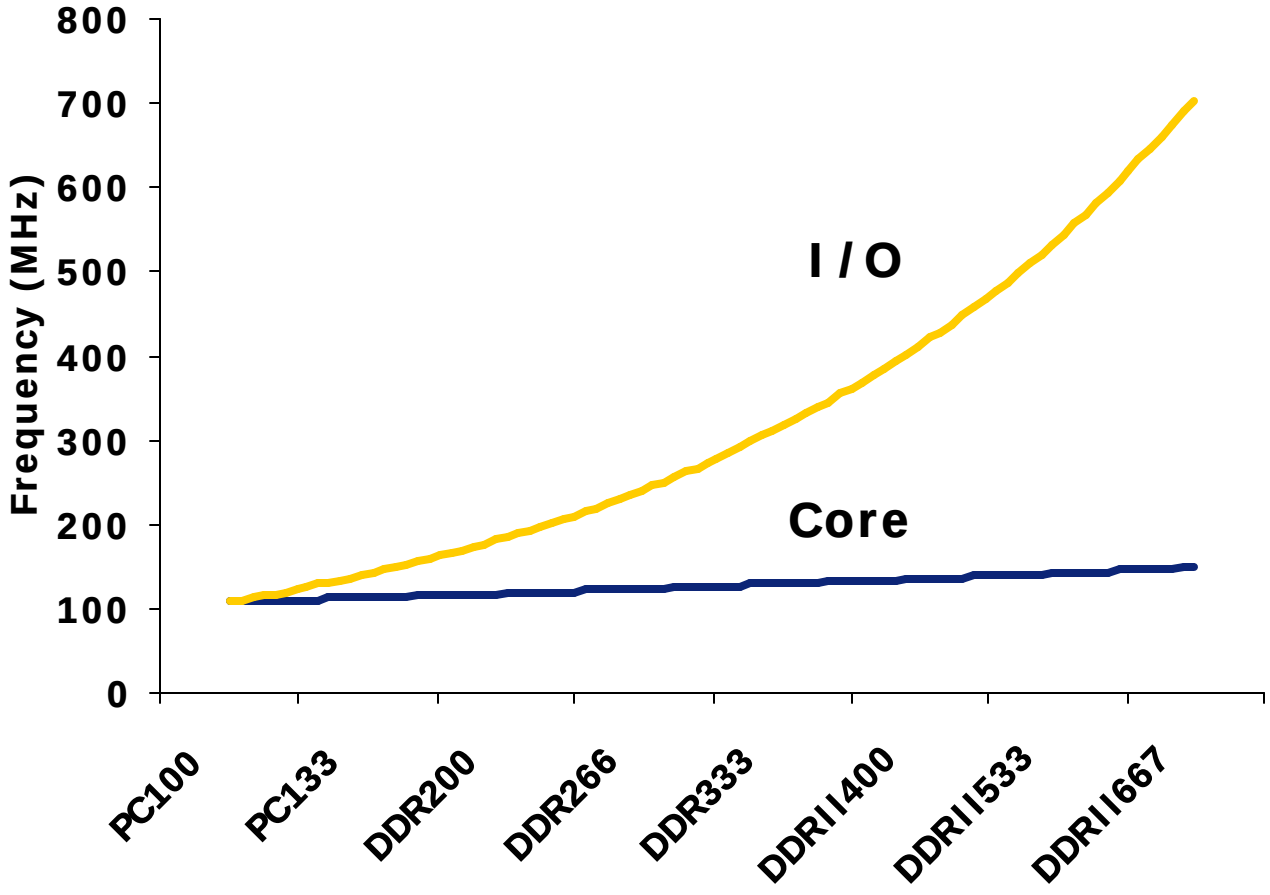
Desktop Performance

- **Challenge:**
  - Always increase the bandwidth
  - Never increase the cost
  - Power dissipation is becoming a challenge
- **Solution:**
  - Architecture must migrate at each technology transition
  - Lower operating voltage
  - Improve signaling
  - Design of memory channel requires intensive engineering
    - Collaboration of system designer and memory supplier is important

Techniques For Increasing Bandwidth

- **Burst modes (SDR, DDRI, DDRII, etc.)**
  - Improves command saturation; tailored to cache lines
  - Inexpensive to implement
- **Multiple strobe edges**
  - Basis of double data rate
- **Prefetching (2n, 4n, etc.)**
  - Pipelining data; minimum WRITE burst
  - Fairly inexpensive die cost; saves power in core
- **Increased core speed**
  - Column-to-column cycle time
  - Gradual improvements; total power reduction higher priority
- **Improved termination techniques**
  - On-die termination for DDRII

Bandwidth vs. Core Speed Trend



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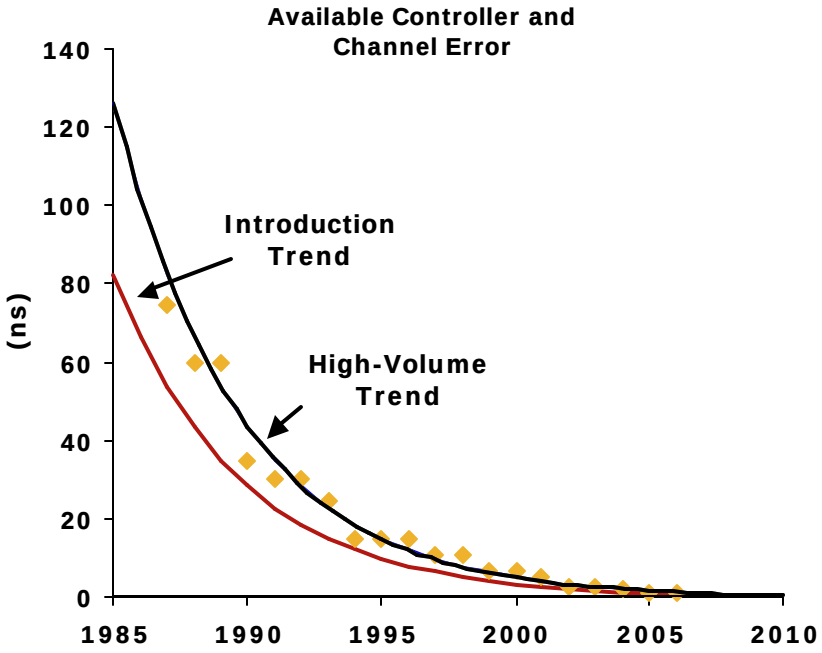
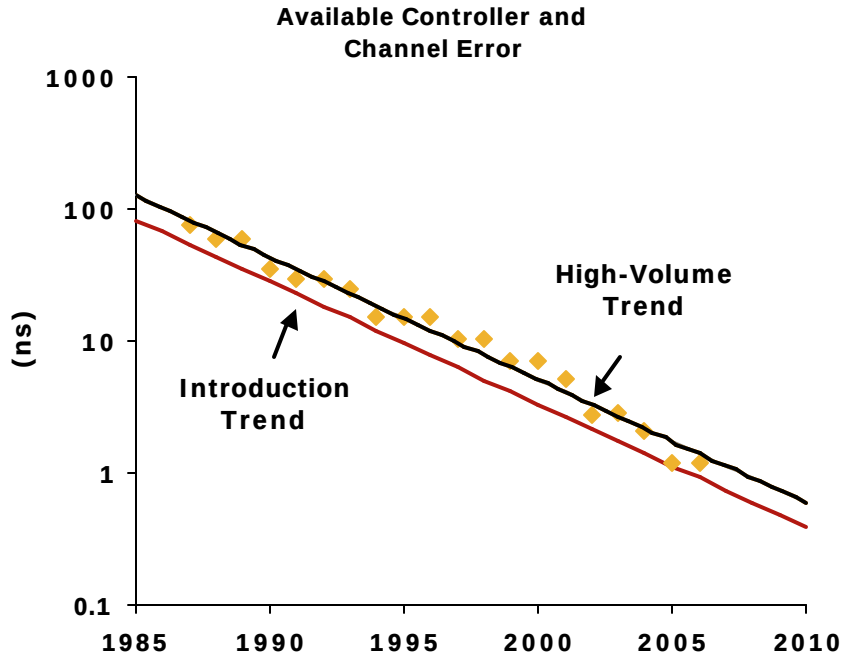
Faster Data Rates Require More Engineering of Signaling and Physical Design



Linear Scale



Logarithmic Scale

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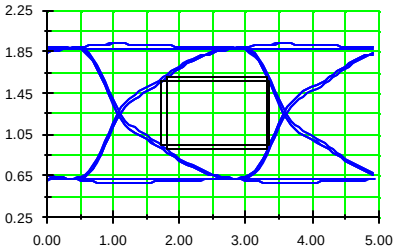
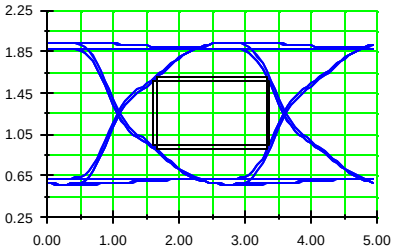
Multidrop Desktop Environment is a Signaling Challenge

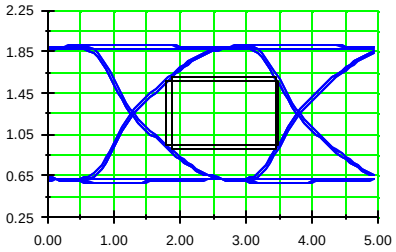
Slot 1 DD
ISI=43 ps Apert2=1.5 ns SlewR=0.73 V/ns



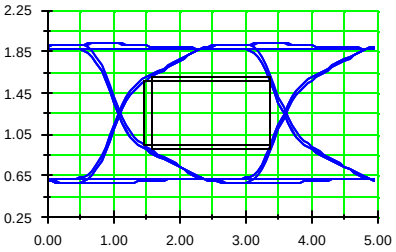
Slot 1 DS
ISI=42 ps Apert2=1.65 ns SlewR=0.88 V/ns



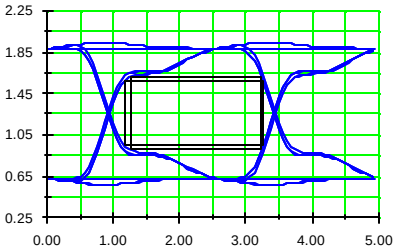
Slot 2 DD
ISI=52 ps Apert2=1.58 ns SlewR=0.79 V/ns



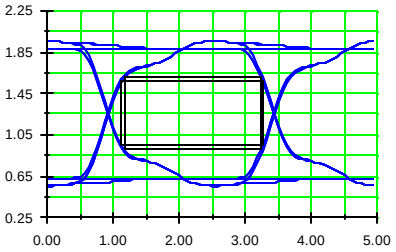
Slot 2 DS
ISI=33 ps Apert2=1.78 ns SlewR=1.1 V/ns



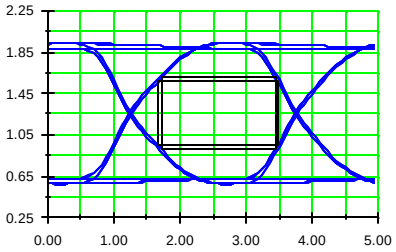
Slot 1 SD
ISI=32 ps Apert2=1.97 ns SlewR=1.59 V/ns



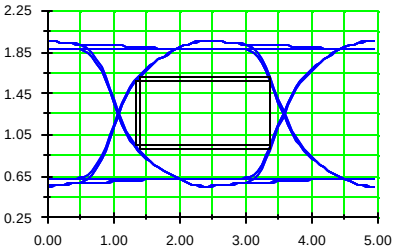
Slot 1 SS
ISI=19 ps Apert2=2.05 ns SlewR=1.75 V/ns



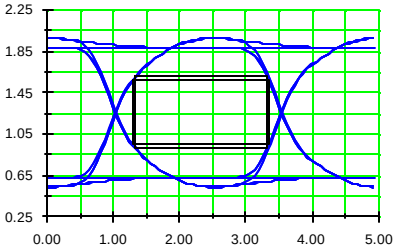
Slot 2 SD
ISI=42 ps Apert2=1.72 ns SlewR=0.95 V/ns



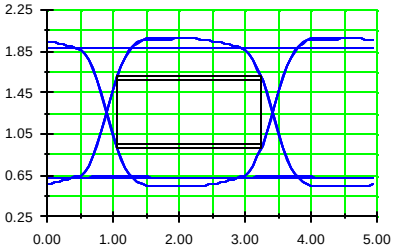
Slot 2 SS
ISI=19 ps Apert2=1.96 ns SlewR=1.41 V/ns



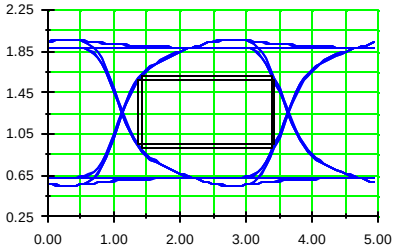
Slot 1 Dx
ISI=16 ps Apert2=1.97 ns SlewR=1.4 V/ns



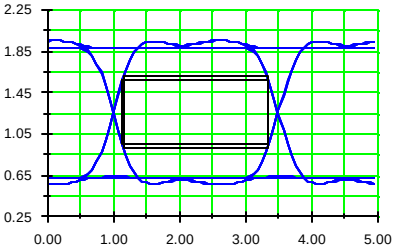
Slot 1 Sx
ISI=5 ps Apert2=2.16 ns SlewR=2.09 V/ns



Slot 2 xD
ISI=19 ps Apert2=1.98 ns SlewR=1.48 V/ns



Slot 2 xS
ISI=4 ps Apert2=2.18 ns SlewR=2.22 V/ns



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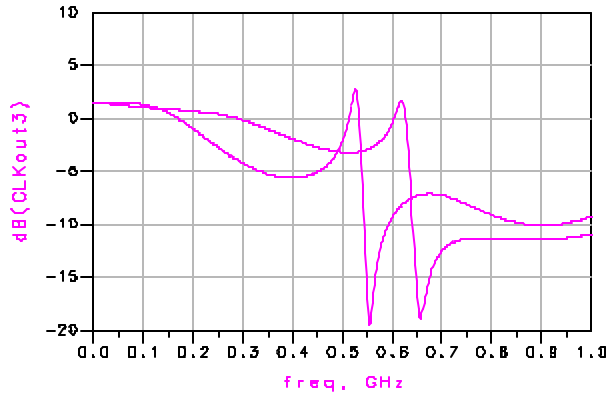
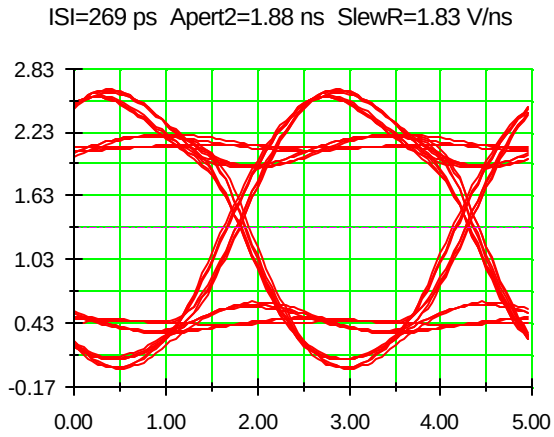
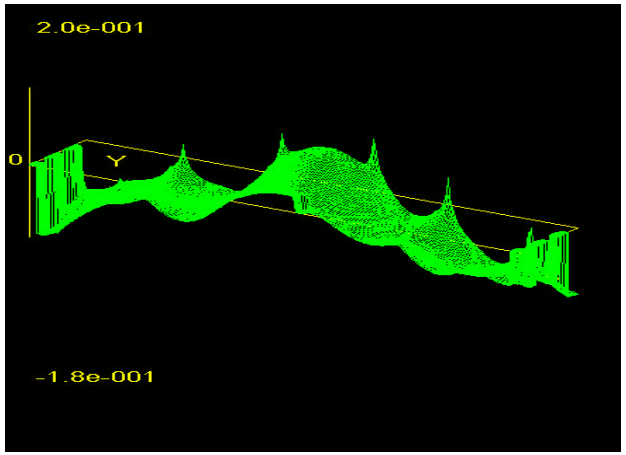
Platform Analysis



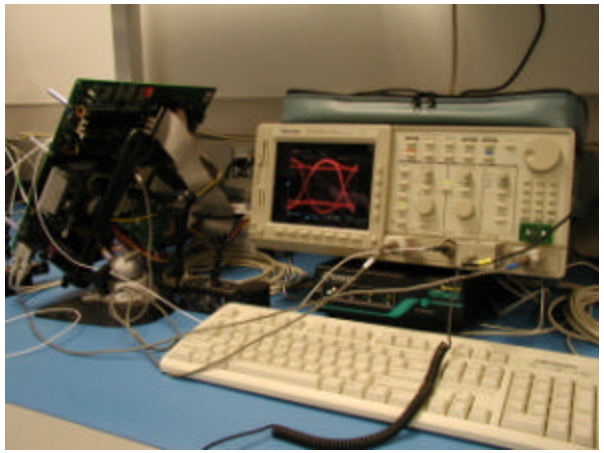
Frequency Domain



Time Domain



Reference Plane Analysis



Hardware Analysis

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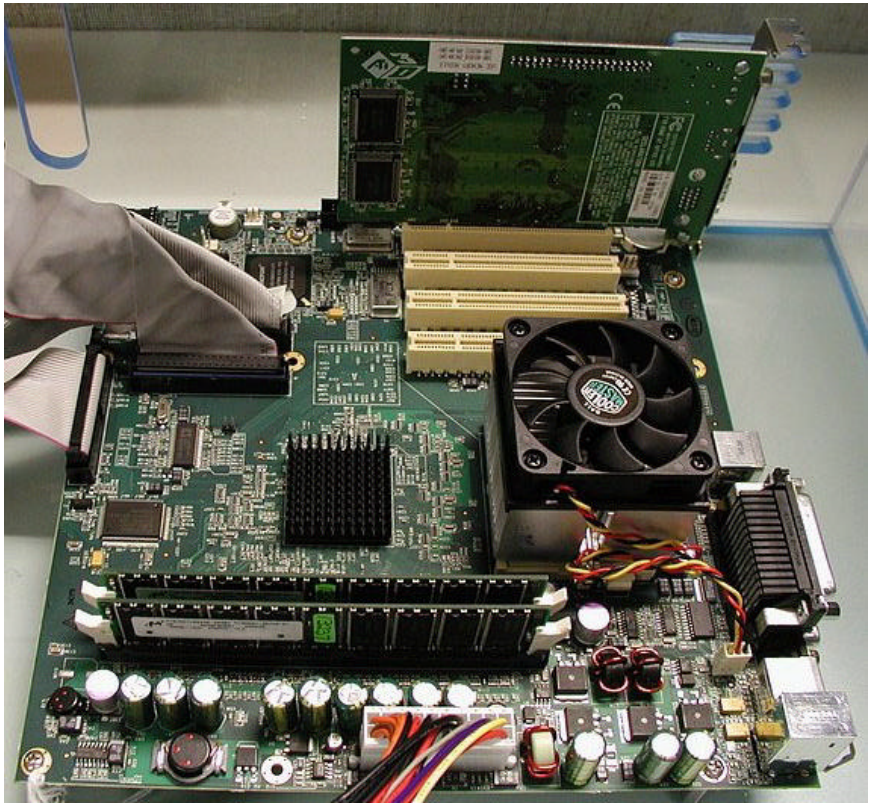
Micron DDR Technology Hardware Demos



- **DDR333 Server**
  - 4-RDIMM system
- **DDR400 Desktop**
  - 2-UDIMM system
- **DDRII Desktop**
  - 533 Mb/s
  - 2-UDIMM system
  - Signal analysis demonstration

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Summary

- End-use applications for memory have changed
- Diverse applications have different types of memory performance needs
- Memory innovation is required
- System designs have become more challenging
- Close collaboration of the system designer and memory supplier is necessary
- Enjoy VTF!

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